REMARKS

It is noted that, during a telephone interview with Examiner Sarkar, it was determined that the Office Action mailed on November 29, 2005 contained certain errors that needed correction, and that the present Office Action, mailed on January 3, 2006, would replace and supercede the November 29, 2005 Office Action and would restart the time for response. Accordingly, the present Amendment is in response to the January 3, 2006 Office Action, and the applicants assume that the November 29, 2005 Office Action has been superceded and is moot, and that its time period for response is no longer running.

It is noted that claims 24-26 are objected to but would be allowable if rewritten in independent form.

Claims 16-20, 22, 23 and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsue, *et al.* (U.S. Patent Number 6,483,142 - hereinafter Hsue '142). Claim 21 rejected under 35 U.S.C. 102(b) as being anticipated by Hsue, *et al.* (U.S. Patent Number 6,512,260 - hereinafter Hsue '260). In view of the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 16-29, a dual damascene interconnection structure with a metal-insulator-metal includes a via level intermetal dielectric and a trench level intermetal dielectric which are sequentially stacked on a substrate. A dual damascene interconnection is formed in the via-level intermetal dielectric and the trench-level intermetal dielectric. A metal-insulator-metal capacitor is formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer and an upper electrode.

Hsue '142 discloses dual damascene patterns including trenches 162 and vias 160 formed in insulator 158 and insulator 138, respectively, which are used for Cu wires 148a and 148b (see Hsue '142, column 6, lines 22-25). A capacitor 132 including a conducting wire 126a, a flat insulator 128a and upper electrode 130a is formed between insulator 138 and insulator 116. Thus, the Cu wire 148b in the trench 162 and via 160 is formed in the insulator 158 and the insulator 138, while the capacitor is formed between the insulator 138 and the insulator 116.

Therefore, Hsue '142 fails to teach or suggest that a dual damascene interconnection structure with a metal-insulator-metal capacitor includes a dual damascene interconnection formed in a via-level intermetal dielectric and a trench-level intermetal dielectric, and a metal-

insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric, as claimed in claims 16-29. Instead, in Hsue '142, the capacitor 132 is formed between the insulator 138 having the vias 160 and the insulator 116, rather than between the insulator 158 having trench 162 of the dual damascene structure and the insulator 138 having the via 160 of the dual damascene structure.

Hsue '142 fails to teach or suggest these elements of the invention set forth in claims 16-29. Specifically, Hsue '142 fails to teach or suggest that a dual damascene interconnection structure with a metal-insulator-metal capacitor includes a dual damascene interconnection formed in a via-level intermetal dielectric and a trench-level intermetal dielectric, and a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric, as claimed in claims 16-29. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 16-20, 22, 23 and 27-29 under 35 U.S.C. 102(b) as being anticipated by Hsue '142, is respectfully requested.

Hsue '260 discloses dual damascene patterns including trenches 142 and vias 140 formed in an insulator 138, and a capacitor 132 formed between insulator 138 and insulator 116.

Therefore, Hsue '260 fails to teach or suggest that a dual damascene interconnection structure with a metal-insulator-metal capacitor includes a dual damascene interconnection formed in a via-level intermetal dielectric and a trench-level intermetal dielectric, and a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric, as claimed in claims 16-29. Instead, in Hsue '260, the dual damascene patterns including trench 142 and via 140 are formed in a single insulator 138, and the capacitor 132 is formed between insulator 138 having the damascene patterns and insulator 116.

Hsue '260 fails to teach or suggest these elements of the invention set forth in claims 16-29. Specifically, Hsue '260 fails to teach or suggest that a dual damascene interconnection structure with a metal-insulator-metal capacitor includes a dual damascene interconnection formed in a via-level intermetal dielectric and a trench-level intermetal dielectric, and a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric, as claimed in claims 16-29. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claim 21 under 35 U.S.C. 102(b) as being anticipated by Hsue '260, is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all

claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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